IN THE SPECIFICATION:

Please correct paragraph **[0023]** at page 6, line 3 to read:

Referring to FIG. 2, the process for fabricating image sensor 200 begins with the formation of a field insulating layer 202. Layer 202 may be formed on a field area of semiconductor substrate 201 and more specifically on a single crystalline silicon substrate. Field insulating layer 202, which ensures electrical insulation between unit pixels, may comprise a field oxide layer that may be formed on **[[substrate 101]]** **substrate 201** using a Shallow Trench Isolation (STI) process. It should be understood, however, that alternative oxidation techniques, such as LOCOS (LOCalized Oxidation of Silicon), may also be used to practice the invention. A unit pixel including a photodiode 203 of a photodetector is then formed on an active area of the semiconductor substrate 201.

Please correct paragraph **[0026]** at page 7, line 7 to read:

Formation of the third interconnect and the second Inter-Metal Dielectric may then be pursued using the same techniques discussed in the previous paragraph. That is, a third interconnect 208 is formed on the second dielectric 207 so as to be positioned above the first interconnect 204. Construction of the third interconnect 208 is then followed by deposition of a third dielectric layer 209, as shown in FIG. 2. Similarly, the **[[third dielectric 208]]** **third dielectric 209**, which ensures electrical insulation between adjacent layers, may be subsequently planarized using conventional planarization techniques, thereby completing the formation of the second IMD layer.